

Atty. Docket No. 02986.P035

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of:

John M. Beardslee, et al.

Application No. 09/724,585

Filed: November 28, 2000

For: METHOD AND SYSTEM FOR
DEBUGGING AN ELECTRONIC SYSTEM

Examiner: Thangavelu, K.

Art Unit: 2123

Confirmation No. 7620

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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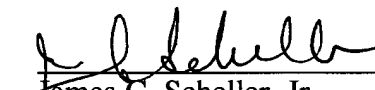
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/16, 2005


James C. Scheller, Jr.
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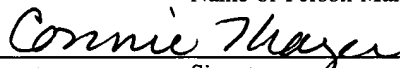
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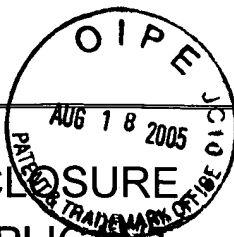
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			Application Number	09/724,585	
			Filing Date	11/28/2000	
			First Named Inventor:	John M. Beardslee	
			Art Unit	2123	
Examiner Name	Thangavelu, K.				
Attorney Docket No.	02986.P035				
Sheet	1	of	7		

U.S. PATENT DOCUMENTS						
Exmnr Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		US- 6,587,995	B1	07/01/2003	Duboc et al.	
		US- 6,779,145	B1	08/17/2004	Edwards et al.	
		US- 6,785,854	B1	08/31/2004	Jaramillo et al.	
		US- 6,789,217	B2	09/07/2004	Slaugh et al.	
		US- 6,791,352	B2	09/14/2004	Verdoorn et al.	
		US- 6,795,963	B1	09/21/2004	Andersen et al.	
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		US- 6,822,474	B2	11/23/2004	Chaudhari	
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		US- 6,826,717	B1	11/30/2004	Draper et al.	
		US- 6,839,654	B2	01/04/2005	Röllig et al.	
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		US- 6,859,892	B2	02/22/2005	Bolding et al.	
		US- 6,868,376	B2	03/15/2005	Swoboda	
		US- 6,894,530	B1	05/17/2005	Davidson et al.	

FOREIGN PATENT DOCUMENTS								
Exmnr Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
		WIPO	00/043884	A1	07/27/2000	Wenzel et al.		
		WIPO	01/063434	A1	08/30/2001	Barry		
		WIPO	01/071876	A1	09/27/2001	Ricchetti et al.		

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		US- 6,895,365	B2	05/17/2005	Voorhees et al.	
		US- 6,895,372	B1	05/17/2005	Knebel et al.	
		US- 6,904,577	B2	06/07/2005	Schubert et al.	
		US- 2004/0111252	A1	06/10/2004	Burgun et al.	
		US- 2004/0181385	A1	09/16/2004	Milne et al.	
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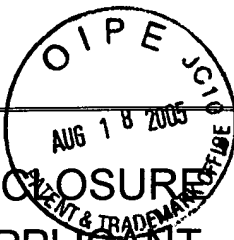
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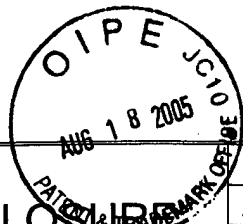


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				Examiner Name	Thangavelu, K.
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		Ableidinger et al., "Multi-Core Embedded Debug for Structured ASIC Systems", DesignCon 2004, February 2004, 23 pgs.			
		"Actel Corporation, "Actel Silicon Explorer II - User's Guide", March 2004; cover page, page ii and pp.3-43.			
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		Altera Corporation, "SignalTap II Features", http://www.altera.com/products/software/products/quartus2/verification/signalatap2/sig-feature_descriptions.html , June 2005, pp. 1-4.			
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		First Silicon Solutions, Inc., "Technical Data for ISA-ACTEL51 In-Target System Analyzer for Actel Core8051 Microcontroller Cores", http://www.fs2.com , June 2005, 2 pgs.			

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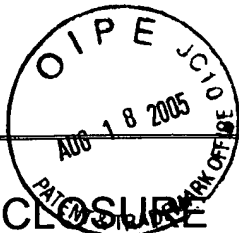
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		First Silicon Solutions, Inc., "Technical Data for ISA-ARM System Analyzer for ARM Processors and Cores", http://www.fs2.com , June 2005, 2 pgs.			
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		First Silicon Solutions, Inc., "Technical Data for FS2 On-Chip Logic Navigator System for Actel FPGA Devices", http://www.fs2.com , June 2005, 2 pgs.			
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Art Unit	2123
Examiner Name	Thangavelu, K.
Attorney Docket No.	02986.P035

Sheet

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of

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		First Silicon Solutions, Inc., "Preliminary Technical Data for FS2 MED System for SoC Multi-Core Embedded Debug", http://www.fs2.com , February 2004, 2 pgs.	
		First Silicon Solutions, Inc., "Technical Data for ISA-M8051EW In-Target System Analyzer for Mentor Grphics M8051EW Synthesizable Microcontroller Core", http://www.fs2.com , June 2005, 2 pgs.	
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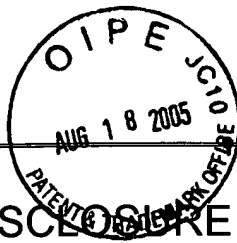
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		S2C Inc., "IP Porter Introduction", http://www.s2cinc.com/aaipi3.asp , June 2005, 9 pgs.	
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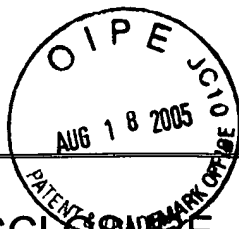
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		Xilinx, Inc., "ChipScope Pro Software and Cores User Guide", UG029, Version v7.1, February 2005, 122 pgs.	
		Yang et al., "Extraction Error Modeling and Automated Model Debugging in High-Performance Low Power Custom Designs", Date Conference 2005, March 2005, 6 pgs.	

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